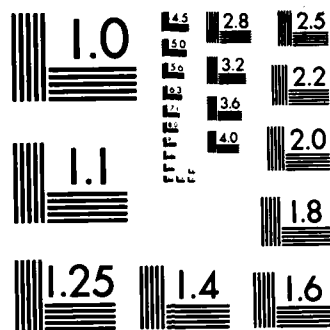END

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER	2. GOVT ACCESSION NO. *AD-A131 925*	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Surface and Interfacial Properties of $Ga_{0.47}In_{0.53}As$ Alloys		5. TYPE OF REPORT & PERIOD COVERED Final Report April 1 '82 to March 31 '83
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) H. H. Wieder		8. CONTRACT OR GRANT NUMBER(s) N00019-82-C-0204
9. PERFORMING ORGANIZATION NAME AND ADDRESS University of California, San Diego Electrical Engineering & Computer Sciences Dept. C-014, La Jolla, CA 92093		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Air Systems Command Washington, DC 20361, Code AIR 310B		12. REPORT DATE July 26th. 1983
		13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Office of Naval Research, Resident Representative La Jolla (Q-043) University of Calif., San Diego La Jolla, CA 92093		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Gallium Indium Arsenide; Semiconductor Surface and Interfacial Properties; Dielectric-Compound Semiconductor Interfaces.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

See page ii.

AD A131925

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Final Report

April 1st, 1982 to March 31st, 1983

Surface and Interfacial Properties of $Ga_{0.47}In_{0.53}As$ Alloys

Contract: N00019-82-C-0204

Naval Air Systems Command

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Abstract

High frequency C-V measurements and quasi-static gate-controlled galvanomagnetic measurements have confirmed theoretical predictions that the surface Fermi level of $Ga_{0.47}In_{0.53}As$ is pinned by lattice defect-related surface states at 0.55 eV above the valence band edge.

The total density of the donor and acceptor centers, related to these defects, is two to three orders smaller than those of InP and the respective barrier heights of n and p-type $Ga_{0.47}In_{0.53}As$-metal contacts are consistent with the equilibrium surface Fermi level of Al_2O_3 as well as other dielectric-$Ga_{0.47}In_{0.53}As$ interfaces.

Introduction

The ternary alloy $Ga_{0.47}In_{0.53}As$ is receiving an increasing attention[1,2] from researchers and technologists primarily because its fundamental physical properties provide some important real and potential advantages for the construction of discrete and integrated circuit optical and electronic components which combine near infrared sensors, compatible with low loss, low dispersion optical fibers with high speed field effect transistors or heterojunction transistors on the same semi-insulating (SI) InP substrate. The lattice constant of $Ga_{0.47}In_{0.53}As$ matches exactly that of InP.

Among the favorable material properties of $Ga_{0.47}In_{0.53}As$ are its direct room temperature fundamental bandgap, $E_g(300°K) = 0.75$ eV, its low electron effective mass, $m_n^* = 0.041\ m_0$, its large energy separation of 0.53 eV between the Γ and L-point conduction band minima and its high electron mobility, $u_n = 10^4 cm^2/V\text{-sec}$ (for $n \simeq 10^{15} cm^3$).

Very little information is, as yet, available concerning the surface and interfacial properties of $Ga_{0.47}In_{0.53}As$. This topic represents the main emphasis of the investigation described in this report. A detailed evaluation of this alloy is desirable within the context of a systematic appreciation of the surfaces of III-V compound semiconductors in general and those of the ternary alloy system $Ga_{0.47}In_{0.53}As$, in particular. The technological application of these materials for the construction of insulated gate field effect transistors requires a thorough understanding of the surface and dielectric-semiconductor interfaces of these materials. The trend towards a decrease in the size and scaling down of transistor parameters in order to increase their speed as well as place a larger number of transistors on the same chip emphasizes the role of surface and interfacial properties over those of the same bulk crystalline materials.

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An understanding of the inherent surface properties of these materials is also needed in order to develop appropriate methods for passivating such devices and integrated circuits in order to impede or retard the degradation induced by the chemical reaction of the ambient environment on the exposed surfaces of these alloys.

Metal-Semiconductor Barriers

Among the earliest experimental investigations of the surface and interfacial properties of the $Ga_{0.47}In_{0.53}As$ alloys are those concerned with their metal-semiconductor barrier heights, ϕ_B. This is usually called a Schottky barrier although overwhelming evidence is now available that Schottky's model[3] of a metal-semiconductor interface is not applicable to any III-V compound semiconductors. This model predicts that $\phi_B = \phi_m - x$ where ϕ_m is the work function of the metal contact relative to the vacuum level and x is the electron affinity of the semiconductor measured from the conduction band edge, at the surface, to the vacuum level. However, ϕ_B does not depend on ϕ_m for any III-V semiconductors. In fact the changes in ϕ_B observed experimentally are usually due to metallurgically-induced interfacial anomalies rather than abrupt interfaces. Using Au electrodes on various $Ga_xIn_{1-x}As$ layers from x = 0 to x = 1, Kajiyama et al.[4] deduced the barrier height ϕ_{Bn} of the n-type alloys from measurements made on their reverse saturation currents. For $Ga_{0.47}In_{0.53}As$ they found $\phi_{Bn} \simeq 0.23$ eV. Subsequently, Morgan and Frey[5] determined $\phi_{Bn} \simeq 0.19$ eV from similar measurements. However, experimental measurements made at the Naval Ocean Systems Center as well as at UCSD indicated that a variety of different metal-n-$Ga_{0.47}In_{0.53}As$ interfaces, including Au, did not yield zero barrier heights, the contacts appeared ohmic probably because of a complex alloying interfacial

process between the metallic contact and the $Ga_{0.47}In_{0.53}As$. Attempts to deposit a thin metallic interdiffusion barrier have not been successful thus far. For that reason we investigated, first, the barrier height of p-type $Ga_{0.47}In_{0.53}As$ and proceeded to deduce therefrom the barrier height of the n-type material. These investigations were performed by UCSD graduate student J. Veteran[6] at NOSC. Using various metal contacts to p-type $Ga_{0.47}In_{0.53}As$ she found that consistently reliable contacts can be made with Al electrodes; although the quality of the planar diodes varied somewhat it was possible to derive the barrier height by means of current vs. voltage (I-V) and capacitance vs. voltage (C-V) measurements as $\phi_{Bp} \simeq 0.55$ eV. Since $\phi_{Bn} < E_g - \phi_{Bp}$ it follows that $\phi_{Bn} < 0.2$ eV in fair agreement with the earlier quoted measurements of ϕ_{Bn}.

It is clear that such a low barrier height with a relatively soft reverse characteristic makes n-type $Ga_{0.47}In_{0.53}As$ unsuitable for use in metal-semiconductor field effect transistors (MESFET). However, provided that the dielectric-semiconductor interfacial characteristics are favorable, i.e. the density of interface states is low enough, it does not prevent the use of this material for insulated gate field effect transistors (MISFET). Since the Fermi level might be pinned in the vicinity of the conduction band edge, in analogy to InP, this should allow its displacement over a substantial portion of the bandgap, towards the valence band edge provided that no other high density of interface states are present within it. We assume here, implicitly, that the barrier is determined by interface states and not by the classical constraints given by Schottky.

Consider the energy band diagram shown in Figure 1 of an n-type depleted III-V compound semiconductor at equilibrium in zero applied voltage, $V_g = 0$; ϕ_{Bn} is the energy interval between the conduction band edge at the surface,
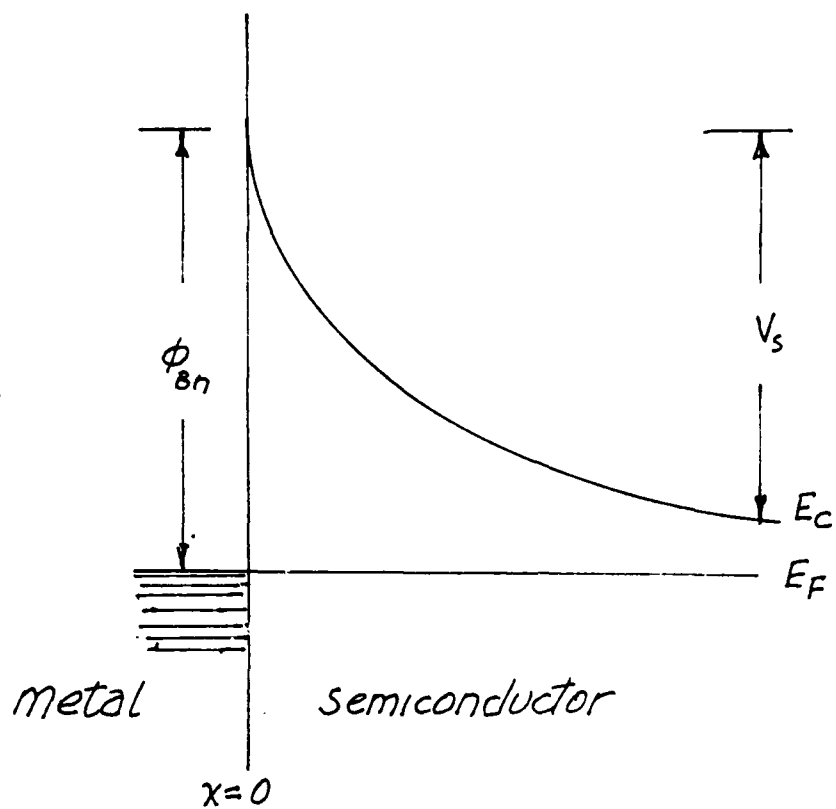
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Figure 1   Energy band diagram of n-type semiconductor
with a surface depletion region.

$x = 0$, and the bulk Fermi level, E_F. Thus $\phi_{Bn} = V_s + E_F$ where V_s, the surface potential is the potential difference between E_{cs}, the conduction band edge at the surface, and E_c that within the bulk of the semiconductor. We assume that in analogy to GaAs and InP the $Ga_{0.47}In_{0.53}As$ surface is depleted prior to the deposition of the metal contact and that the latter does not produce any substantial charge readjustment in the semiconductor surface layer because its equilibrium value is determined, essentially by charges trapped in surface acceptor states. Thus, it might be expected that the energy of such traps as well as their density might play an important role in "pinning" the Fermi level. In such a metal-semiconductor structure it might be assumed that the equilibrium position of the Fermi level is coincident with the trapping level if the surface traps are the dominant interfacial phenomena which determine ϕ_{Bn}.

The Surface Fermi Level

The conventional surface band diagram[7] of a metal-insulator-semiconductor (MIS) structure is shown in Figure 2; it is employed to describe the silicon-silicon-dioxide-metal (MOS) interfaces. At equilibrium, the gate voltage, V_g, expressed in terms of the potential drop across the oxide, V_{ox}, the surface potential, V_s, the potential barrier between the Fermi level of the metal and the conduction band of the oxide, ϕ_M, the electron affinity, x, of the semiconductor, is

$$V_g = V_{ox} - (\phi_M - x) + V_s + (E_g/2 - V_B) \qquad (1)$$

where the bulk potential, V_B, is the potential difference between the intrinsic energy level and the bulk Fermi level. If the contribution of
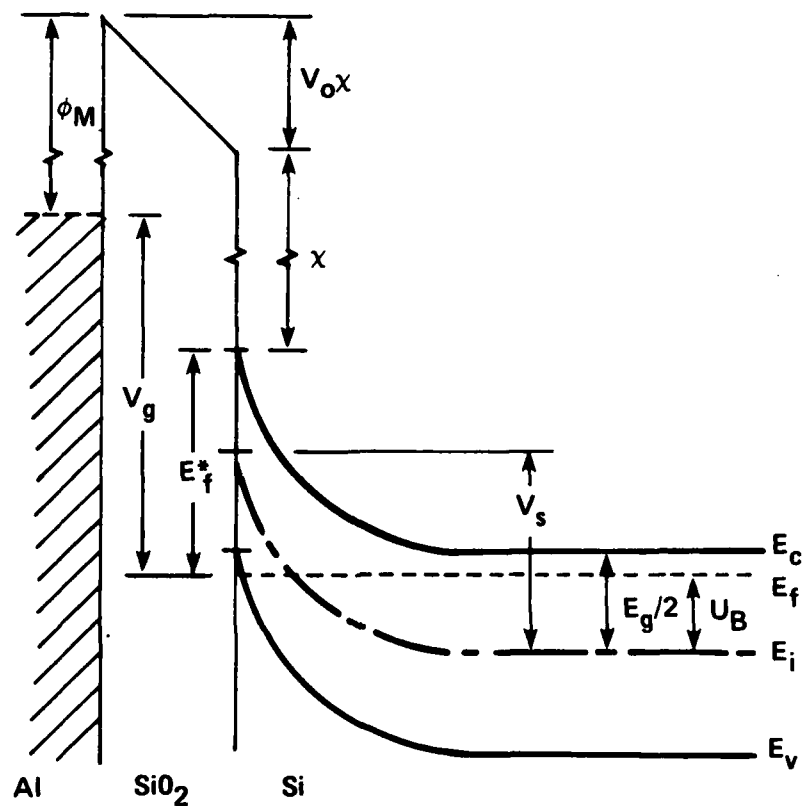
Figure 2   Band diagram of a depleted n-type silicon
            MOS capacitor.   Parameters are described
            in text.

surface or interface states is negligible then the equilibrium surface Fermi
level, E_F^*, for $V_g = 0$ can be expressed, in terms of Figure 2, as

$$E_F^* = V_s + E_F = (\phi_M - \chi) - V_{ox} \qquad (2)$$

Note that E_F^* is the energy interval between the conduction band edge at the
surface and the bulk Fermi level, thus, its definition as the surface Fermi
level is justified. Furthermore, in terms of Figure 1 note that $E_F^* = \phi_{Bn} =$
$V_s + E_F$; therefore the term surface Fermi level might be usable for bot
metal-semiconductor and dielectric-semiconductor interfaces. Just as f 'he
III-V compound metal-semiconductor interfaces, the MIS III-V compound
interfaces are not dependent on the characteristics of the metal electroue or
on the rather ill defined electron affinity of the semiconductors. The
explicit dependence of E_F^* on $(\phi_M - \chi)$ in eq.(2) suggests that if the same
relation is applicable to other semiconductors having dielectric layers other
than SiO_2 then changing the dielectric or the metal gate ought to affect E_F^*.
However, experimental measurements made on a variety of III-V compound
semiconductors with various types of homomorphic and heteromorphic dielectric
layers indicate that, at least to first order E_F^* is not dependent on the type
of dielectric or metal used to produce MIS structures. If surface states
produce the experimentally observed $E_F^* = V_s + E_F$ and the band bending produced
by these states is inherent in the surface properties of the semiconductor
then one might expect that E_F^* would be independent of $(\phi_m - \chi)$; provided that
chemical or metallurgical interactions have a negligible effect on these
surfaces then E_F^* should be the same on "free" surfaces, dielectric-
semiconductor interfaces and metal-semiconductor interfaces. This is the type
of phenomenological behavior we might also expect for $Ga_{0.47}In_{0.53}As$ and have

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attempted to find experimentally.

A substantial quantity of experimental data and its interpretation is now available on the surface and interfacial properties of GaAs and InP surfaces. These might be summarized in the following statements:

1. The surface Fermi level, E_F^* of GaAs and InP "free surfaces" produced by the exposure of clean (110)-cleaved surfaces to oxygen is essentially the same as ϕ_{Bn} or ϕ_{Bp} produced by depositing on these surfaces as little as a fractional monolayer of a metallurgically non-reactive metal.

2. MIS structures made of these III-V compounds on which synthetic dielectric layers are deposited at temperatures T < 300°C or on which anodic oxides are grown by wet electrochemical anodization or plasma anodization yield E_F^* values in good agreement with those measured on oxidized surfaces (in accordance with item #1 above).

3. In ultrahigh vacuum cleaved (110) surfaces these compounds are at flatband; i.e. $E_F^* = E_F$. X-ray photoemission spectroscopic measurements (XPS) illustrate the evolution of band bending hence the formation of a surface potential and consequently the change in E_F^* with increasing surface oxygen chemisorption. Increasing the oxygen exposure finally leads to a diffusion limited saturation of E_F^* which is the same as that of the same semiconductor surfaces exposed to the ambient environment. As a rule, a fractional monolayer of oxygen is sufficient to "pin" the surface Fermi level.

We assume that other III-V semiconducting compounds, including the ternary alloy $Ga_{0.47}In_{0.53}As$, have an oxidized surface layer due to their exposure to the ambient environment and the interface between this oxide layer and the appropriate semiconductor surface determines, to a large extent, the

Figure 3   Dependence of fundamental bandgap of $Ga_xIn_{1-x}As$ alloys on the molar fraction, x, of GaAs. Barrier height is energy difference between conduction band minima and As vacancy-related trapping states.

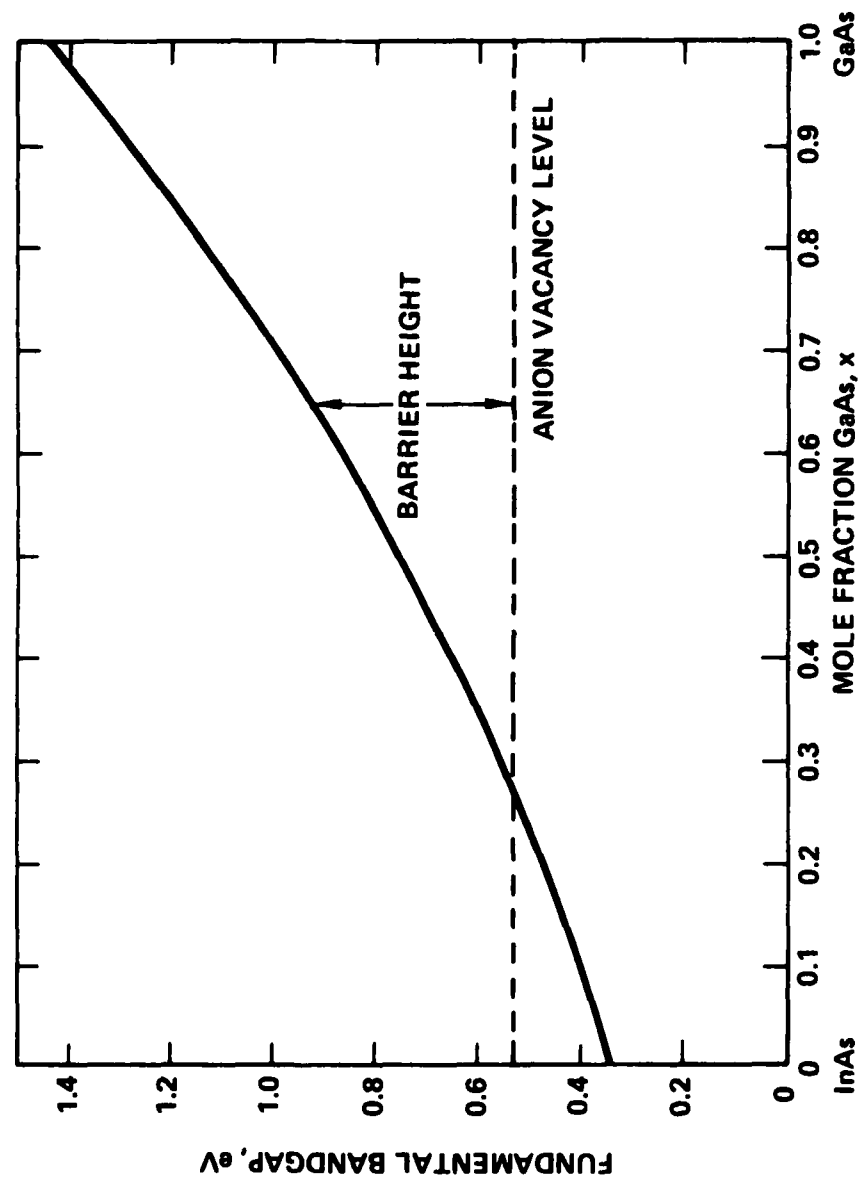exposure to the ambient environment and the interface between this oxide layer and the appropriate semiconductor surface determines, to a large extent, the energy level of E_F^*. It is presumed that the oxidation process creates extrinsic surface states and that it is the energy and density of these states that determine E_F^* and that these surface states are localized on oxidation-induced surface defects. Correlations have been established between the XPS measurements made on "free" surfaces and C-V and I-V measurements made on MIS structures and metal-semiconductor diodes of GaAs and InP. Unfortunately, no XPS measurements have been made, as yet, on $Ga_{0.47}In_{0.53}As$ because no bulk crystals are available, at present, of this material and since cleaving requires massive crytalline specimens and only cleaving of (110) substrates in ultrahigh vacuum has produced thus far "unpinned", i.e. $E_F^* = E_F$ surfaces such measurements have to be deferred for the present.

Fortunately, other experimental data is available which illustrates the specific similarities between the surface and interfacial properties of $Ga_{0.47}In_{0.53}As$ and those of the binary III-V alloys and suggests that the same basic physical mechanisms are operative or at least are closely related. Consider Figure 3 which shows[8] the composition dependence of the fundamental bandgap $E_g(300°K)$ of the ternary alloy system $Ga_{0.47}In_{0.53}As$. For p-doped GaAs (x = 1) as well as for x = 0.47 the measured metal-semiconductor barrier height is the same as the surface Fermi level, $\phi_{Bn} = E_F^* \doteq 0.55$ eV, relative to the valence band maximum.

We assume, herewith, that the surface Fermi levels of p-type $Ga_{0.47}In_{0.53}As$ alloys are pinned by As defect-related surface states whose energies are located at ϕ_{Bp}. The crystal lattice of these alloys is considered, in accordance with Figure 4 to be made up on two interpenetrating sublattices displaced along their body diagonals. The As sublattice is
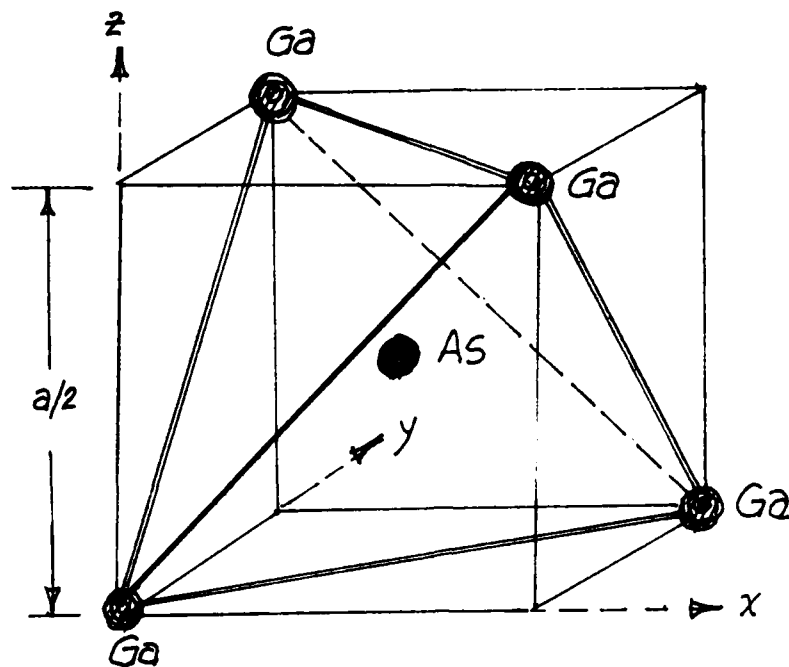
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Figure 4   The GaAs lattice is a cubic face centered lattice

of Ga atoms and a corresponding lattice of As atoms.

The local vector of the GaAs atoms can be expressed as:

$$d = n_1 a_1 + n_2 a_2 + n_3 a_3$$

where n_1, n_2 and n_3 are integers and

$$a_1 = \frac{a}{2} (011) \qquad a_2 = \frac{a}{2} (010) \qquad a_3 = \frac{a}{4} (111)$$

the local vector of the As atoms is:

$$d' = d + s \qquad s = \frac{a}{4} (111)$$

each As atom is in a tetrahedral environment of Ga atoms

and vice-versa. Inversion symmetry exchanges the As and

Ga atoms in the GaAs lattice. Similar relations apply

for the InAs lattice. It is presumed that in the case of

$Ga_x In_{1-x} As$ the In atoms have a random distribution within

the Ga sub-lattice.

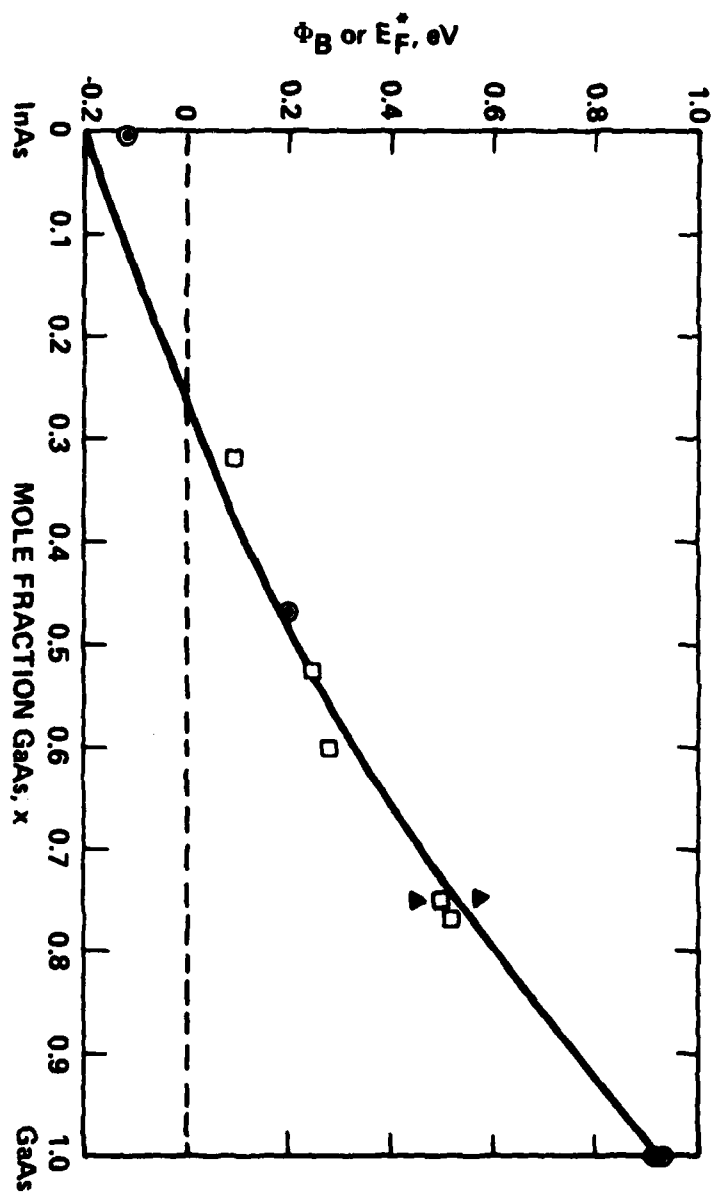Figure 5   The barrier heights ϕ_{Bn} and ϕ_{Bp} as well as the equilibrium surface Fermi level E_F^* dependence on the molar fraction x of GaAs in InAs.

ordered except for defects (not considered in this context) and the In atoms occupy random positions within the Ga sublattice. We assume, furthermore, that the density of the As defects is not a function of relative atomic fraction x of the cations and is represented by the parallel line $E_F^* = 0.55$ eV above the valence band edge in Figure 3 while E_g is a function of x. Since the barrier height of n-type $Ga_{0.47}In_{0.53}As$ is expected to be

$\phi_{Bn} = E_g(x) - \phi_{Bp}$ it follows that the energy difference between $E_g(x)$ and ϕ_{Bp} in Figure 3 should yield ϕ_{Bn}. Figure 5 shows that this is indeed the case and that the experimental data is in excellent agreement with these aassumptions which require that the surface states at $E_F^* = 0.55$ eV have both donor-like and acceptor-like characteristics such as might be attributed to As vacancies which might have either of three charge states: neutral, positively charged or negatively charged and thus account for the observed surface depletion from $x \simeq 0.33$ to $x = 1$. At $x = 0.33$ E_g crosses E_F^* and the surfaces of n-type $Ga_{0.47}In_{0.53}As$ with $x < 0.33$ are accumulated (ϕ_{Bn} has a negative value) while the surfaces of the p-type alloys are inverted. It is thus reasonable to expect from the evidence presented in Figure 5 that Fermi level pinning of p-type $Ga_{0.47}In_{0.53}As$ in the vicinity of its conduction band edge should allow surface inversion by a gate voltage applied to an appropriate MIS structure as well as the construction of inversion-mode field effect transistors operating in a manner analogous to those of silicon inversion-type MOSFET or InP inversion-type MISFET and these phenomena and the devices based upon them confirmed this prediction. However, in order to promote a better understanding of the surface properties of $Ga_{0.47}In_{0.53}As$ a theoretical foundation is required based on first principles.

Daw and Smith[9] have made ab initio calculations of bound-state energy levels of the (110) surface related As vacancies in $Ga_{0.47}In_{0.53}As$, using a

virtual crystal approximation, with the tight binding parameters of GaAs and InAs averaged compositionally. They found that the highest filled As vacancy level increases only slightly (≤ 0.2 eV) relative to the $Ga_{0.47}In_{0.53}As$ valence band edge between $x = 0$ and $x = 1$. Thus, to first order the assumption that the energy level attributed to an As vacancy appeared to be justified qualitatively.

However, Allen and Dow[10] have challenged this view. They pointed out that vacancies are energetically less stable and thermodynamically less probable than antisite defects, that vacancies are likely to be filled or react otherwise with adatoms and that some quantitative discrepancies appear between the surface vacancy model and experimental data beyond the uncertainty of the theory. They calculated the dependence of ϕ_{Bn} on x assuming the presence of antisite defects. Their theoretically derived barrier height dependence on the molar concentration of GaAs in InAs is in better agreement with experimental measurements than those which involve As vacancies, however, their model has not been used as yet to drive $\phi_{Bp}(x)$.

It is tempting to assume that if Fermi level pinning in $Ga_{0.47}In_{0.53}As$ alloys is due, principally, to antisite defects then the relative concentration of such defects would be a function of the molar fraction x. Allen and Dow[11], based on their theoretical calculations, predict the antisite defect As_{Ga} to produce a donor level, $E_{ds} = 0.7$ eV, and the antisite defect In_{As} to produce a donor level, $E_{ds} = 0.65$ eV. Thus, the partial substitution of one for the other, assuming that their surface state densities are nearly the same, is likely to have a small effect on the measured ϕ_{Bp}, in agreement with experimental observations.

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Dielectric-$Ga_{0.47}In_{0.53}As$ Interfaces

C-V measurements made on two-terminal GaAs MIS structures indicated that the Fermi level is pinned near midgap by a high density of interface states[12]. This allows only a limited excursion of the Fermi level from its equilibrium position near the center of the fundamental bandgap to the vicinity of the valence band edge. Depletion mode MISFET made of GaAs have, therefore, a limited dynamic range and the high density of interface states per unit energy per unit area, N_{ss}, which have long time constants reduce their transconductances at low frequencies; in fact the transconductance in the quasi-static regime, $g_m \simeq 0$. In contrast with GaAs, InP has its Fermi level pinned near the conduction band edge. This was determined on a large number of different MIS structures using various homomorphic and heteromorphic dielectric layers. The interface state densities of InP-dielectric interfaces are[13] more than one order of magnitude smaller than those of GaAs near its midgap. Almost the entire bandgap is available for the displacement of the Fermi level from its equilibrium $V_g = 0$ position; MISFET made of n-type InP exhibit only a small decrease in g_m at frequencies less than 10^2 Hz and do respond in the quasi-static regime.

There were no a-priori indications that n-type $Ga_{0.47}In_{0.53}As$ MIS structures would behave like MIS n-type InP except for the earlier stated metal-semiconductor measurements which indicated that its Fermi level also appeared pinned near the conduction band[14]. Preliminary C-V measurements indicated qualitatively a low density of interface states using either SiO_2 or Al_2O_3 dielectric layers for making the MIS structures. No evidence of Fermi level pinning was found in these MIS structures. It was evident, however, that depletion mode MISFET were feasible and, given the lack of Fermi level pinning, that inversion mode MISFET could be made[15] of n-type

$Ga_{0.47}In_{0.53}As$. Such devices were demonstrated to be feasible in both n-type InP and $Ga_{0.47}In_{0.53}As$. However, no such devices can be made as yet either in n-type or p-type GaAs. Furthermore, surface accumulation can be induced in both n-type InP and $Ga_{0.47}In_{0.53}As$; no such accumulation is feasible in GaAs MIS structures. Depletion mode $Ga_{0.47}In_{0.53}As$ MISFET were described by Gardner[16] to have very favorable properties and a variety of dielectric layers[17-19] have been used, thus far, to make depletion mode as well as inversion mode MISFET. C-V measurements made subsequently on MIS structures with an Al_2O_3 dielectric layer and Al electrodes showed that the surfaces of $Ga_{0.47}In_{0.53}As$, under the dielectric layers, were slightly accumulated for $V_g = 0$ in qualitative agreement with the experimental measurements of Tell et al.[20] obtained on plasma anodized dielectric layers grown on n-type $Ga_{0.47}In_{0.53}As$. An evaluation of the quasi-static properties using galvanomagnetic techniques has been made by the writer in collaboration with Dr. Donald P. Mullin. It represents the paper presented orally at the 10th Conference on the Physics and Chemistry of Smiconductors, Santa Fe, N.M. in Feb.(1983) by D. Mullin; this paper will be published in the Proceedings of the Conference in the Journal of Vacuum Science and Technology (1983). It is included in this report as an Appendix.

Results obtained from the gate controlled galvanomagnetic measurements can be summarized in the following manner: E_F^* of virgin MIS structures is pinned at ~0.2 eV below the conduction band minimum (0.55 eV above the valence band maximum) of $Ga_{0.47}In_{0.53}As$, in agreement with the experimentally measured and theoretically calculated barrier height of metal-$Ga_{0.47}In_{0.53}As$ diodes provided that such MIS structures are made by the deposition of the Al_2O_3 dielectric layers at low temperatures. Annealing at 120°C for 16 hours or growth of the dielectric layers at temperatures in excess of 300°C reduces the

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density of interface states by more than a factor of two, to the order of $10^{11}cm^2eV$; it eliminates Fermi level pinning, thus allowing the Fermi level to be displaced over a substantial portion of the fundamental bandgap. The dielectric-$Ga_{0.47}In_{0.53}As$ interface behaves more nearly like that of InP than that of GaAs and has electronic properties which are analogous in many respects to those of the $Si-SiO_2$ interface.

Densities of Interface States

It may be assumed that the specific energy levels, E_{as} and E_{ds}, are not dependent on the type or density of impurities in the bulk and that band bending accompanied by the displacement of the Fermi level proceeds primarily by changes in their respective densities, N_{as} and N_{ds} produced by increasing chemisorption of oxygen. Nedoluha[21] has calculated these surface state densities for InP from the XPS data of Spicer et al.[22] of the Fermi level displacement as a function of oxygen exposure with the assumption that E_{as} = 0.83 eV and E_{ds} = 1.31 eV relative to the valence band maximum (VBM). He found that the Fermi level is pinned by N_{as} = 1.41 x $10^{14}/cm^2$ and N_{ds} = 1.47 x $10^{14}/cm^2$. Similar values can be deduced from data derived from measurements made on n-type, p-type and SI InP MIS structures in the following manner:

The total density including both ionized and unionized surface donors and acceptors, respectively, N_{ds} and N_{as}, can be calculated from the equilibrium charge balance equation, $Q_s + Q_{ss}$ = 0 at V_g = 0, where the total surface charge, Q_s, includes as appropriate, the space charge, the inversion charge or accumulation charge and Q_{ss} is the charge trapped on surface states. If the ionized donor and acceptor densities are respectively, N_{ds}^+ and N_{as}^- then with Q_{ss} = N_s/a it follows that $N_s = N_{ds}^+ - N_{as}^-$ and

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$$N_s = N_{ds}\{1 + \exp[(E_F + V_s - E_{ds})/kT]\}^{-1}$$

$$- N_{as}\{1 + \exp[(E_{as} - E_F - V_s)/kT]\}^{-1} \tag{3}$$

With all energies referenced to the VBM, E_{ds} = 1.31 eV, E_{as} = 0.833 eV and with N_s, E_F and V_s obtained from C-V and galvanomagnetic measurements made at room temperature introduced in eq.(3) for n-type, p-type and SI InP leads to simultaneous equations which can be solved for N_{ds} and N_{as}. Since little is known about the spin degeneracy factor it has been assumed to be unity in eq.(3). These calculations lead to $N_{ds} \approx 8.66 \times 10^{13}/cm^2$ and $N_{as} \approx 8.60 \times 10^{13}/cm^2$ in fair agreement with the results obtained by Nedoluha[27] on the E_F^* dependence on oxygen exposure.

In a similar manner the density of the donor and acceptor state densities in $Ga_{0.47}In_{0.53}As$ were calculated by means of the data described in the appendix and the following considerations:

$E_{ds} = E_{ds}$ = 0.55 eV above the VBM, $E_F^* \approx 0.15$ eV and E_{FP}^* = 0.57 eV; using eq.(3) this leads to $N_{as} \approx 2 \times 10^{11}/cm^2$ and $N_{ds} \approx 5.7 \times 10^{12}/cm^2$, values considerably smaller than those of InP. It is, therefore, not surprising that moderate annealing techniques can lead to large changes in the surface properties of $Ga_{0.47}In_{0.53}As$.

Conclusions

The results obtained duri..g the phase of research on the surface and interfacial properties of $Ga_{0.47}In_{0.53}As$ clearly indicate that its surface state density near midgap is more than one order of magnitude smaller than that of GaAs that the surface Fermi level in the undoped or n-doped material is pinned a low density of interface states at the Al_2O_3 - $Ga_{0.47}In_{0.53}As$ interface, and that such pinning can be eliminated by low temperatures, moderate annealing procedures.

A substantial amount of work remains as yet, to be done in order to obtain a better understanding and, ultimately, to achieve technological control of the dielectric/semiconductor interfaces of $Ga_{0.47}In_{0.53}As$:

a) The energy dispersion, the time constants and capture cross-sections of surface and interface states and their spatial distribution need to be determined.

b) An unambiguous identification of the type of defects, of the surface states associated with these defects and of defect/impurity interactions.

c) A clarification of the interfacial stereochemistry of the native oxide and of the transition layer between this oxide and the semiconductor.

d) There is a need to extend this work to include the properties of MIS interfaces in accumulation and inversion.

e) Similar investigations need to be performed on p-doped $Ga_{0.47}In_{0.53}As$ layers.

f) Some investigations should be extended to include the surfaces and interfacial properties of the other $Ga_xIn_{1-x}As$, particularly those with the molar fraction $x < 0.3$.

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Surface and interfacial properties of $Ga_{0.47}In_{0.53}As$-Al_2O_3 MIS structures

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Abstract

Field-effect-controlled electrical and galvanomagnetic measurements have been made on transistor-like five-terminal metal insulator semiconductor (MIS) structures using n-type $0.25\mu m$ thick $Ga_{0.47}In_{0.53}As$ epitaxial layers grown on semi-insulating InP substrates. These layers have an electron density, $n = 3.5 \times 10^{16}$ cm^{-3} and a mobility, $\mu_n = 7.5 \times 10^3$ cm^2/V-sec; $0.13\mu m$ thick Al_2O_3 dielectric layers, grown by an RF plasma-assisted low temperature chemical-vapor deposition (CVD) process were employed as gate insulators under $0.01cm^2$ vacuum-deposited aluminum gates.

Hall effect and resistivity measurements were made on such structures and the experimentally observed gate voltage dependent change in resistivity and Hall coefficient of the conducting channel under the gate have been related to the corresponding change in the depletion depth of the surface space charge region. The data were used to derive the density of the surface states and their position within the fundamental bandgap of $Ga_{0.47}In_{0.53}As$.

We find that the surface Fermi level E_F^* of virgin MIS structures is pinned $\sim$ 0.2eV below the conduction band minimum (0.55eV above the valence band maximum) of $Ga_{0.47}In_{0.53}As$, in agreement with the experimentally measured and theoretically calculated barrier height of metal $Ga_{0.47}In_{0.53}As$ diodes. Annealing at 120°C for 16 hours reduces the density of interface states by more than a factor of two and eliminates Fermi level pinning allowing the surface potential to be displaced over a substantial fraction of the fundamental bandgap, in agreement with data derived from C-V measurements made on MIS structures with different types of dielectric layers using different annealing procedures.

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Introduction

A number of papers have appeared in the technical and scientific literature[1-9] which describe galvanomagnetic measurements made on semiconductor thin films or layers grown on insulating or semi-insulating substrates, where surface depletion or accumulation can be controlled by means of a Schottky-barrier gate or a dielectrically insulated gate in such a manner that the gate voltage, V_g effectively controls the depletion depth or the charge in the accumulation layer under the gate. As a result, the apparent resistivity $\rho'(V_g)$ and Hall coefficient $R'_H(V_g)$ are functions of the gate voltage because the effective thickness of the conducting channel or the charge within the channel are functions of V_g. Moreover, it appears that a more detailed characterization of the quasi-static surface and interfacial properties of the dielectric-semiconductor interface of such gate-controlled galvanomagnetic structures is feasible provided that the free-carrier concentration in the channel is assumed to be independent of its thickness and the impurity density of the layer is considered to be constant. This is likely to be the case if the electron mobility measured as a function of gate voltage is invariant with depletion depth. In this context, we attempt to extract from the apparent Hall coefficient and resistivity the true parameters describing the conducting channel and those of the dielectric-semiconductor interface.

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At flatband, for a layer of thickness d_0, the Hall voltage v_{H_0} expressed in terms of the transverse magnetic induction B, the current i, and the Hall coefficient R_{H_0} is

$$v_{H_0} = \frac{R_{H_0} iB}{d_0} = K \left(\frac{R_{H_0}}{d_0} \right) \tag{1}$$

where K is a constant. If this surface is depleted and the depletion depth is δ, then the Hall voltage becomes

$$v_H = K \frac{R_{H_0}}{d_0 - \delta} = K R'_H / d_0 \qquad . \tag{2}$$

Thus, because the conducting channel does not constitute the entire semiconductor layer, we obtain from the measurement of v_H an apparent Hall coefficient R'_H. From equation (2) it follows that

$$\delta = d_0 \left(1 - R_{H_0} / R'_H \right) \tag{3}$$

and by assuming that the depletion approximation is applicable

$$\delta = \left(\frac{2\epsilon_s}{qN_D} \right)^{1/2} \left(|V_s| - \frac{kT}{q} \right)^{1/2} \tag{4}$$

where ϵ_s is the dielectric constant of the semiconductor, q is the charge of the electron, V_s is the surface potential of the n-type

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depleted semiconductor, k is Boltzmann's constant, and T is the temperature. We assume that the layer is sufficiently thick that the depletion depth is limited by the onset of inversion in an insulated-gate structure. The inversion layer itself is not probed by the resistivity and Hall measurements because it is isolated from the conducting channel by potential barriers surrounding each contact as well as by this depletion layer. The maximum depletion depth δ_{max} is reached when the surface potential $V_s = 2 U_B$ where $U_B = 1/q(E_F - E_i)$ is the bulk potential, E_F is the Fermi level, and E_i is the intrinsic Fermi level of the semiconductor. If the term kT/q is neglected in equation (4) then

$$\delta_{max} = \left(\frac{4\epsilon_s U_B}{qN_D} \right)^{1/2} \tag{5}$$

and can be expressed as

$$\delta_{max} = \left(\frac{4\epsilon_s \ kT \ \ln(N_D/n_i)}{q^2 N_D} \right)^{1/2} . \tag{6}$$

where n_i is the intrinsic carrier concentration. The intrinsic carrier concentration was calculated from the relation

$$n_i = (N_c \ N_v)^{1/2} \ \exp \ (- E_g/2kT) \tag{7}$$

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where the conduction band density of states for $Ga_{0.47}In_{0.53}As$ is

$$N_c = 4.831 \times 10^{15} (m_n^*/m_o)^{3/2} T^{3/2} = 2.083 \times 10^{17} \text{ cm}^{-3} \tag{8}$$

with the electron effective mass[10] $m_n^* = 0.041 \ m_o$ and T = 300K. The valence band density of states is

$$N_v = 4.831 \times 10^{15} (m_p^*/m_o)^{3/2} T^{3/2} = 6.351 \times 10^{18} \text{ cm}^{-3} \tag{9}$$

with the hole effective mass $m_p^* = 0.4 \ m_o$ and T = 300K. With a fundamental bandgap of $E_g = 0.75$ eV, $n_i = 6.265 \times 10^{11} \text{ cm}^{-3}$. The intrinsic Fermi level is then

$$E_i = \frac{E_g}{2} - \frac{3kT}{4} \ln\left(\frac{m_p^*}{m_n^*}\right) \tag{10}$$

Thus, the intrinsic Fermi level is $E_i = 0.33$ eV below E_c, the conduction band edge.

The depletion depth $\delta(V_g)$ can be determined from experimental measurements of $R_H'(V_g)$ using equation (3) and the surface potential dependence $V_s(V_g)$ can then be calculated by means of equation (4). If the insulating layer under the gate has a capacitance per unit area $C_i = \epsilon_i/d_i$ where ϵ_i is the dielectric constant and d_i its thickness, then the charge density on the gate is

$$Q_g = C_i (V_g - V_s) \tag{11}$$

In depletion, Q_g is the sum of the space charge density $Q_{sc} = qN_d$ and of the charge density in surface states $Q_s = qN_s$,

$$Q_s = C_i (V_g - V_s) - (2\epsilon_s qN_D V_s)^{1/2} \qquad (12)$$

Therefore $Q_s(V_g)$ can be determined from experimental measurements and the interface state density per unit energy,

$$N_{ss} = \frac{1}{q} \frac{\delta Q_s}{\delta V_s} \qquad (13)$$

can also be calculated. Thus within the limits of the assumptions used here, this is a quasi-static evaluation of N_{ss} within the bandgap of the semiconductor in depletion. This technique has been used to evaluate the surface properties of n-type layers of $Ga_{0.47}In_{0.53}As$ grown epitaxially on semi-insulating InP substrates.

Specimen Preparation and Preliminary Results

The $Ga_{0.47}In_{0.53}As$ layers were grown on semi-insulating InP substrates by liquid-phase epitaxy. The layers were undoped and had typical electron concentrations of 3.4×10^{16} cm^{-3} and room temperature mobilities of about 7500 cm^2/V-sec. The modified van der Pauw-type structure[11,12] shown in Figure 1 was defined by etching through the layer to the semi-insulating substrate. The active region was then thinned to 0.25μm by chemical etching. Prior to the deposition of the gate insulator, the samples were cleaned by sequentially rinsing in warm KOH, H_2O, and dilute HF to remove surface oxides followed by a thorough rinsing in H_2O. The 0.126μm-thick Al_2O_3 dielectric layers were grown in a RF

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plasma-assisted low temperature chemical-vapor deposition system from the reaction of trimethyl aluminum and oxygen.[13] An aluminum gate having an area of 0.01 cm^2 was then evaporated over the dielectric as shown in Figure 1. The processing of these structures was completed by opening holes in the Al_2O_3 over the contact pads, the attachment of a gate lead with a conductive paste and the soldering of the remaining contacts. The surface barrier height, ϕ_{Bn} of $Ga_{0.47}In_{0.53}As$ is ≤ 0.2 eV;[14] therefore it is relatively easy to make ohmic contacts for the current and Hall terminals.

A preliminary measurement of such a structure with zero gate voltage using van der Pauw's[11] method was used to determine the conductivity thickness product (the sheet conductivity)

$$\sigma d = \frac{2 \ln 2}{\pi} (R_1 + R_2)^{-1} f^{-1}(R_1, R_2) \qquad (14)$$

where R_1 and R_2 are the resistances measured between adjacent commutated contacts using a constant current source and f is a function of R_1 and R_2 defined in reference 11. The sheet Hall coefficient R_H/d was determined from the Hall voltage measured between opposite contacts using a typical current of 1.5×10^{-5}A and then commutating the terminals.

Assuming $d_o = 0.25\mu m$, the measurements yield $R_H = 171.5$ cm^3/C, $\sigma = 45.25$ $(ohm-cm)^{-1}$, an electron mobility $\mu = 7769$ cm^2/V-sec and an electron density $n = 3.64 \times 10^{16}$ cm^{-3}. However, this does not represent the values at flatband as the surface of $Ga_{0.47}In_{0.53}As$ is slightly accumulated. This is evident in C-V measurements[15] which suggest the presence of a positive charge in the oxide or the

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presence of surface states which shift the C-V curve to the left of the origin and, therefore, flatband is achieved with an applied negative voltage, V_g = -0.25V. For this value of V_g, R_{H_o} = 212.5 cm^3/C, σ_o = 37.88 (ohm-cm)$^{-1}$, n_o = 2.94 x 10^{16} cm^{-3} and μ = 8035 cm^2/V-sec.

Gate Voltage Dependence of Galvanomagnetic Properties

The gate voltage dependence of the effective Hall coefficient R_H' is shown in Figure 2, curve (a), for a specimen prepared in the configuration illustrated in Figure 1. It shows the qualitatively expected behavior: R_H' increases with V_g in depletion and saturates, presumably in the surface inversion regime. Figure 3, curve (a) shows the depletion depth δ dependence on V_g calculated by means of equation (3) assuming that R_{H_o} = 212.5 cm^3/C. It also shows an ideal $\delta(V_g)$ for values of V_s $\leq$ 2U$_B$, assuming no surface states to be present and δ_{max} calculated by means of equation (6). The difference between the two curves is attributed to the presence of surface states which cause the overall decrease in the $\delta(V_g)$ derived from experimental measurements relative to the ideal curve and is responsible for the inability to deplete the channel to a depth sufficient to produce inversion. The ideal $\delta(V_g)$ and δ_{max} of Figure 3 were used to calculate R_H' and R_H'(max) shown in Figure 2, curve (b). This curve represents the apparent Hall coefficient in the absence of any surface states. It is obvious from curve (b) that the saturation observed in curve (a) is not due to inversion but rather it must be attributed to the presence of a high density of surface states.

Curve (a) in Figure 4 shows the gate voltage dependence of the surface potential calculated by means of equation (4) using the $\delta(V_g)$ data of Figure 3. This data, in conjunction with equations (12) and (13) were used, thereafter, to calculate the surface state density dependence on energy shown in Figure 5, curve (a), which indicates that the Fermi level cannot be displaced beyond $\simeq 0.2$ eV below the conduction band of $Ga_{0.47}In_{0.53}As$, in good agreement with the experimentally measured Schottky barrier height $\phi_{B_n} \simeq 0.21$ eV determined by Kajiyama, et.al.[14]

Curves (b) in Figures 3, 4, and 5 represent the data obtained on the same specimen following annealing in an ambient environment at a temperature of 120°C for a period of 16 hours. Thus, even low temperature annealing can prevent pinning of the Fermi level, as shown in Figure 5, curve (b), which suggests that the density of interface states responsible for pinning the Fermi level is reduced, in comparison with the $N_{ss}(E)$ of the virgin specimen. This is also evident in the $N_{ss}(E)$ data of Kobayashi and Shinoda[16] obtained on an MIS capacitor with an Al_2O_3 dielectric layer grown at 350°C. Their method of deposition of the dielectric layer is apparently sufficient to prevent pinning of the Fermi level; only a small cusp is present at ~ 0.2 eV below the conduction band, at the pinning position of the unannealed specimen. Even more dramatic effects have been obtained on p-type $Ga_{0.47}In_{0.53}As$ MIS capacitors with an SiO_2 dielectric layer by Kaumanns, et.al.[17] They found that annealing at 850°C for three hours in an $AsH_3 + H_2$ environment lowers and broadens the $N_{ss}(E)$ minimum, reducing its value by more than one order of magnitude compared to that of the virgin specimen shown here.

The good agreement between the $N_{ss}(E)$ data obtained by Kobayashi and Shinoda using C-V measurements and that illustrated in Figure 5 derived from galvanomagnetic measurements sugests that, at least, to first order such measurements can be used to obtain quasi-static $N_{ss}(E)$ data, i.e., where all of the surface or interface states respond to the changes in the applied gate voltage. The fair agreement with the data of Kaumanns, et.al., also obtained by C-V measurements, additionally indicates that the nature of the synthetic dielectric layer is not itself a major factor in determining the $N_{ss}(E)$ characteristics which are believed to be, primarily, a function of the $Ga_{0.47}In_{0.53}As$ surface and of its native oxide. It is indicated, however, that the exact details of the dielectric deposition process, presumably including chemical treatment prior to deposition, and subsequent thermal treatment can profoundly affect these results.

Figure 6, curve (a), shows the gate voltage dependence of the effective resistivity ρ' measured by means of van der Pauw's method on the virgin specimen, assuming that the effective thickness is d_o and that it is independent of V_g. Figure 6 also shows in curve (b) that if ρ' is corrected for the appropriate depletion layer thickness from Figure 3, then ρ is essentially independent of V_g. Since it was previously assumed that the ionized donor density is independent of position within the $Ga_{0.47}In_{0.53}As$ layer in the calculation of the depletion depth, it then follows from Figure 6 that the electron mobility is independent of depletion depth. This property of the layers is also supported by profiling of the Hall coefficient and resistivity on other specimens by alternatively performing the galvanomagnetic measurements and chemical etching to thin the

conducting layers. These results showed the electron concentration and mobility to be constant to within a few hundred angstroms of the epilayer-substrate interface.

The Al_2O_3 dielectric used in this study was slightly conductive with a resistivity $\rho_{ox} \geq 5 \times 10^{12}$ ohm-cm. The gate leakage current was monitored during the measurement process and did not exceed a few nanoamps. Since this is less than 0.01% of the typical channel current, the effect of this additional current on the Hall voltage is negligible. This is in contrast to quasi-static C-V measurements on such an MIS structure where leakage currents of this magnitude could seriously affect the measurement.

Summary

Galvanomagnetic measurements on MIS structures as a function of gate voltage have been made on n-type $Ga_{0.47}In_{0.53}As$ epilayers using an Al_2O_3 dielectric. The effective Hall coefficient and resistivity have been used to provide a quasi-static determination of the surface state density within the bandgap. The results agree substantially well with those obtained on similar MIS structures by C-V measurements.

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FIGURE CAPTIONS

Figure 1. Schematic diagram of a symmetrical MIS structure for gal-
           vanomagnetic measurements.

Figure 2. Effective Hall coefficient versus applied gate voltage.
           (a) experimentally determined values, (b) calculated
           value of $R_H^{'}$ assuming no surface states are present.

Figure 3. Gate voltage dependence of the depletion depth (a) prior
           to annealing, (b) after low temperature annealing and
           calculated value of δ assuming no surface states are
           present.

Figure 4. Gate voltage dependence of the surface potential -
           (a) prior to annealing and, (b) after low temperature
           annealing. Also shown is the value of V_s corresponding
           to strong inversion.

Figure 5. The surface state density dependence on energy determined
           by galvanomagnetic measurements·for (a) virgin specimen
           and, (b) the same specimen after low temperature
           annealing.

Figure 6. Effective resistivity versus gate voltage determined
           prior to annealing (curve (a)) and (b) the resistivity
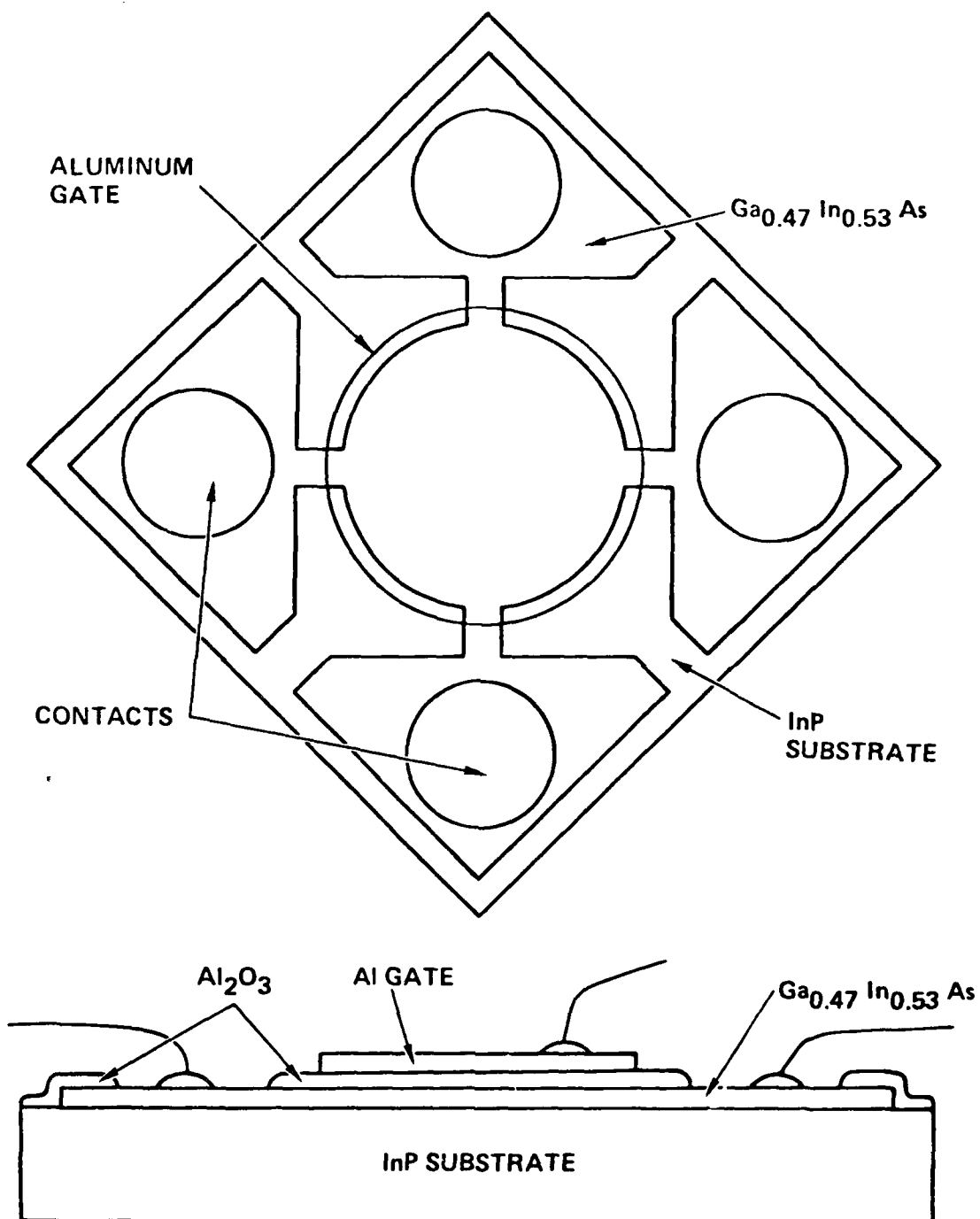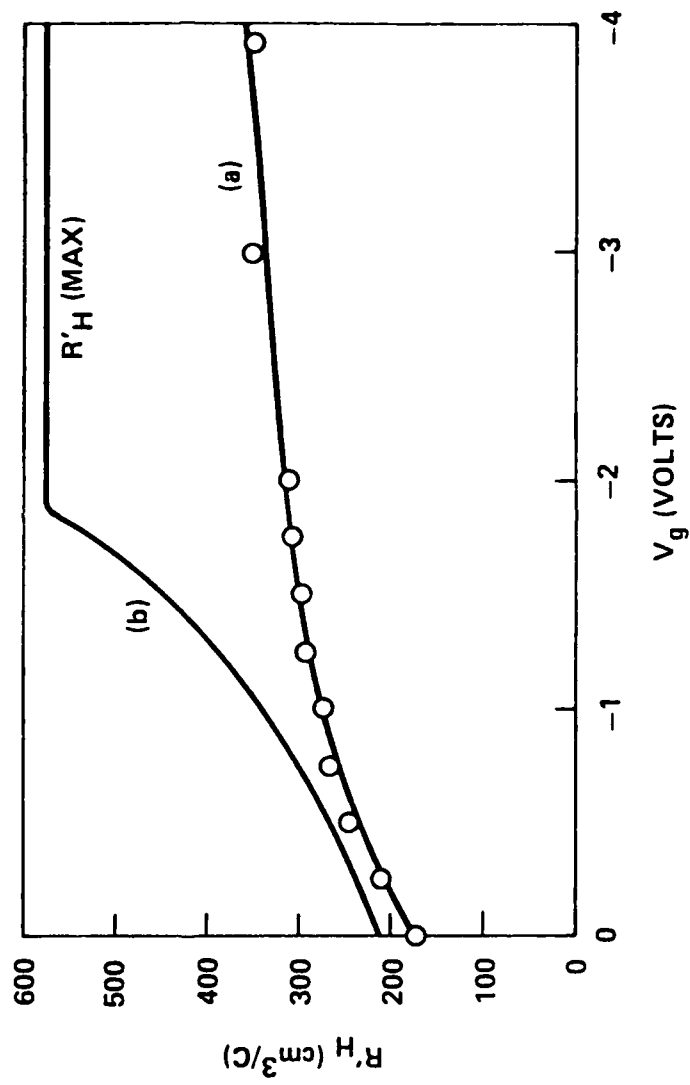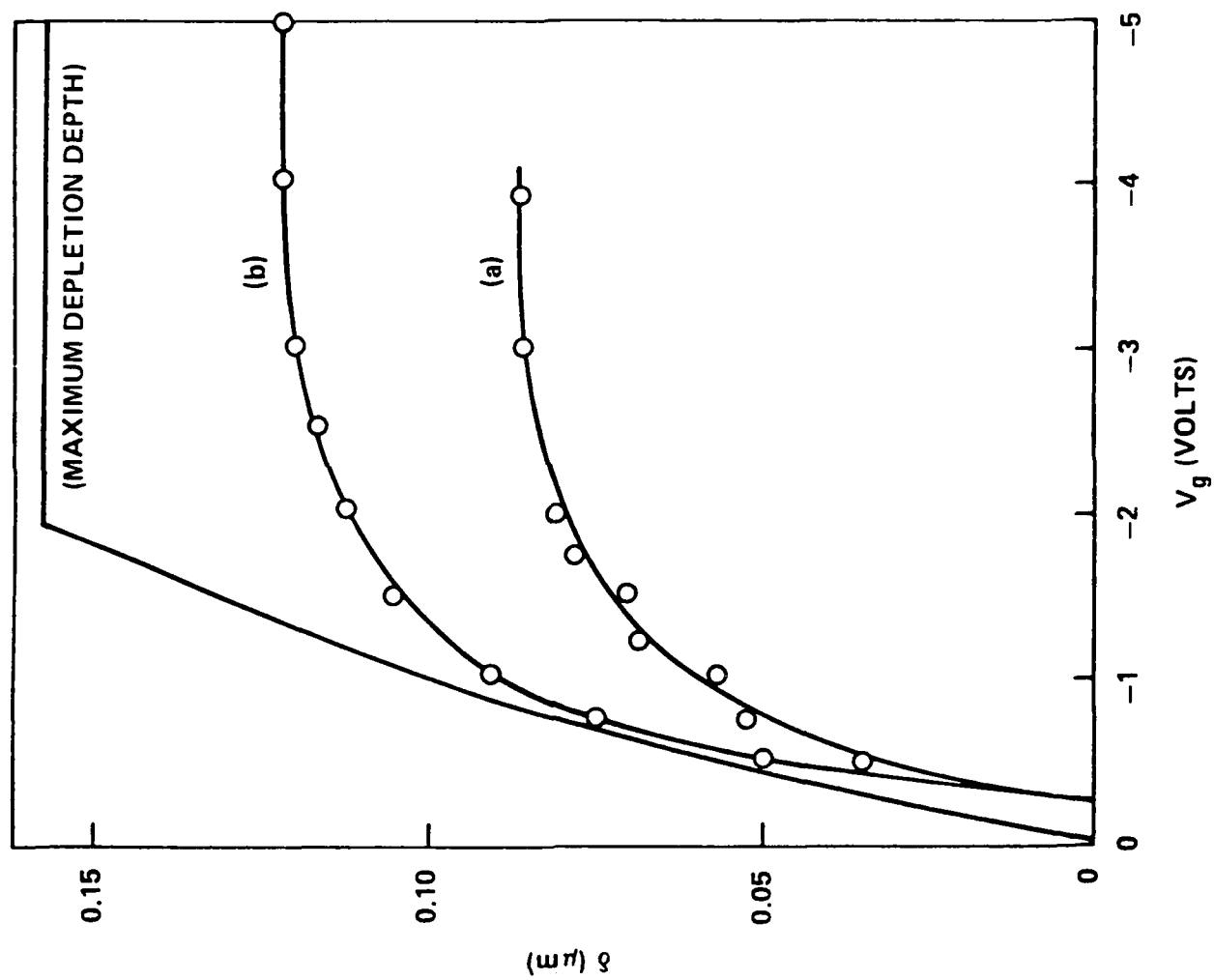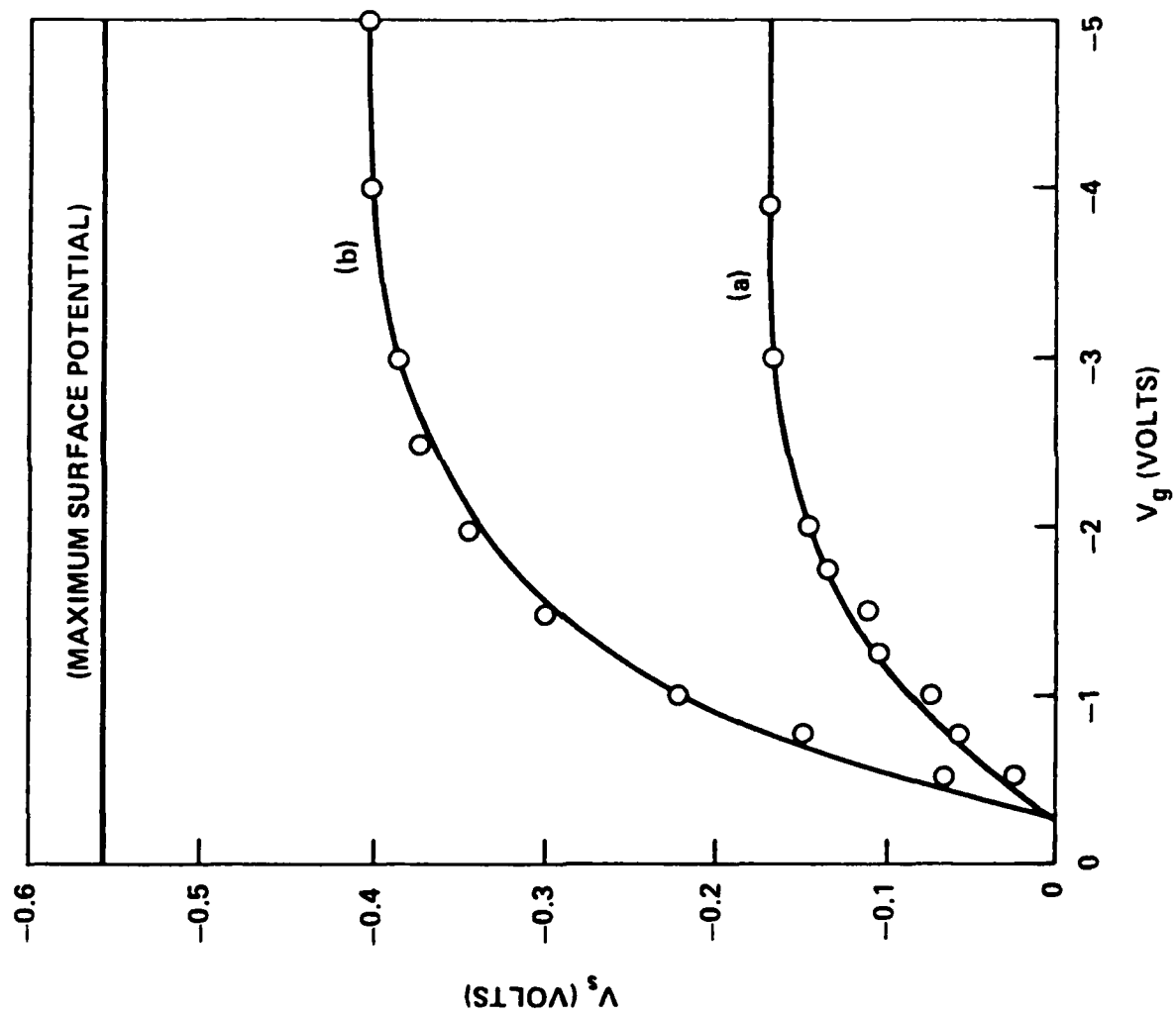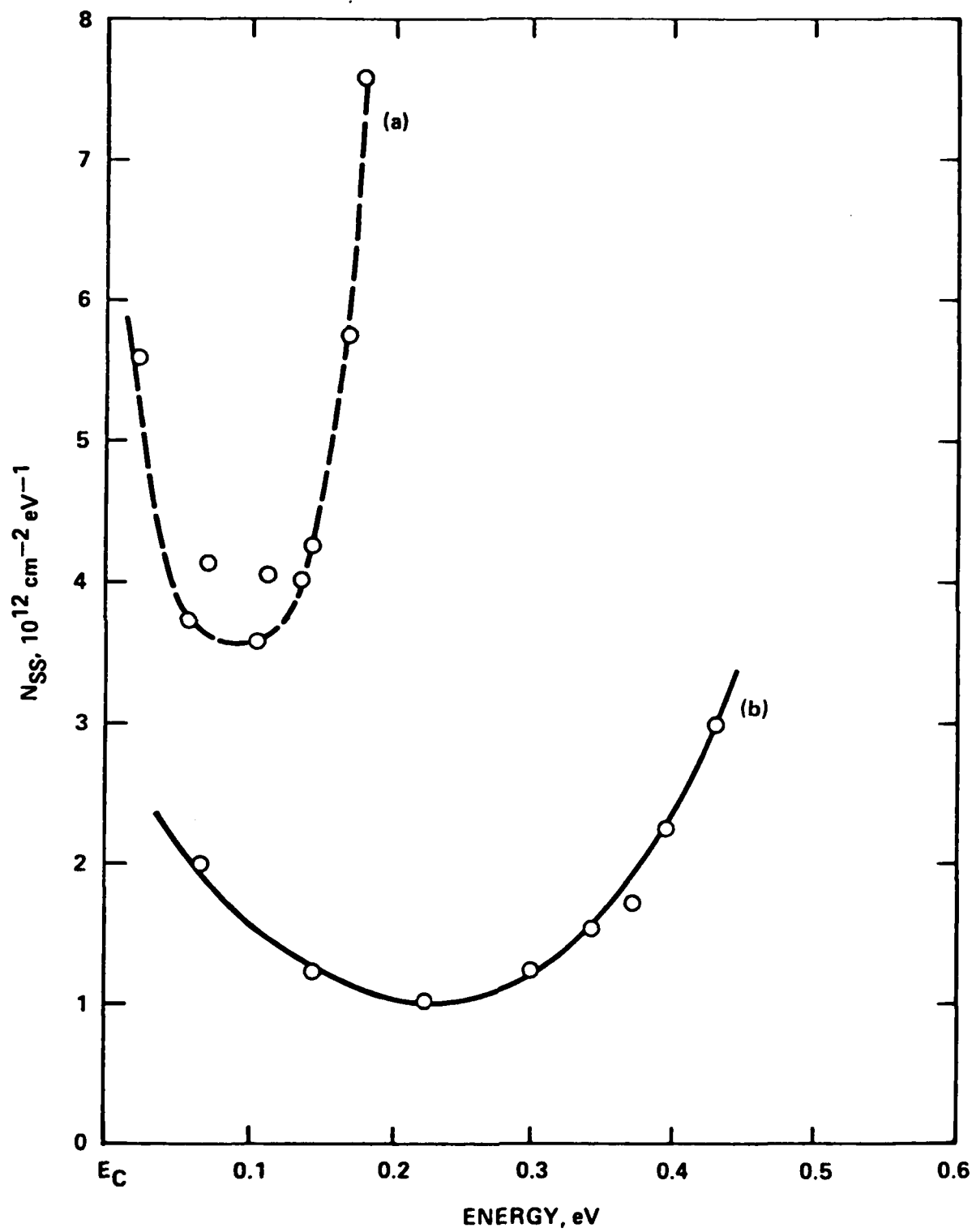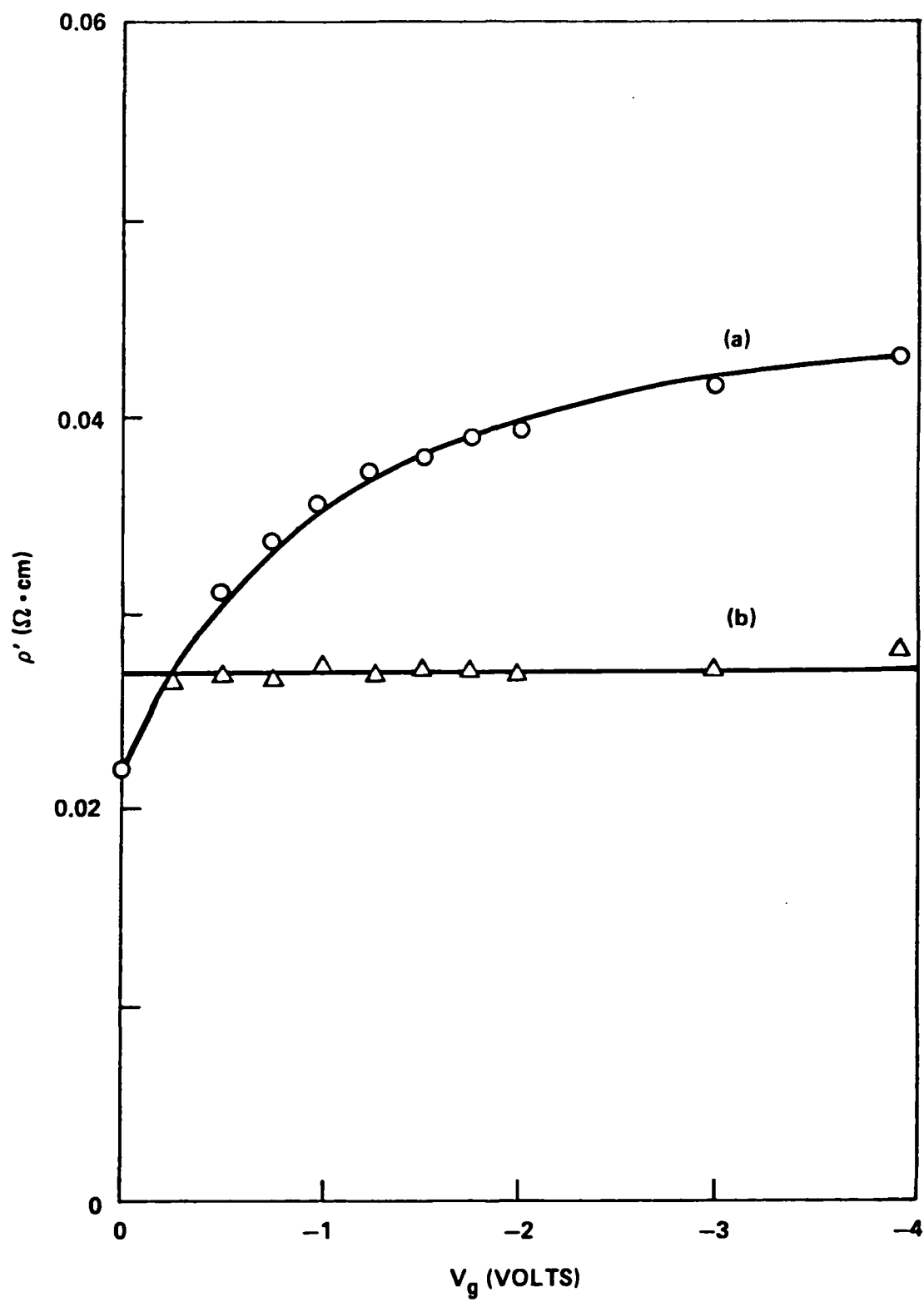   after correction for the depletion layer thickness.

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Figure 1

Figure 2

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Figure 4

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Figure 5

Figure 6

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